

# NN514256 / NN514256A series Fast Page Mode CMOS 256K × 4bit Dynamic RAM

## DESCRIPTION

The NN514256/A series is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 4 bits. The NN514256/A series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN514256/A series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by  $\overline{\text{CAS}}$  which, in essence, acts as an output enable independent of  $\overline{\text{RAS}}$  with very fast  $\overline{\text{CAS}}$  to output access time.

Refresh is accomplished by performing  $\overline{\text{RAS}}$  only refresh cycles, hidden refresh cycles,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit the NN514256/A series to be packaged in a standard 20-pin plastic DIP, 26-pin plastic SOJ, 20-pin plastic ZIP and 24 pin TSOP TYPE I. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

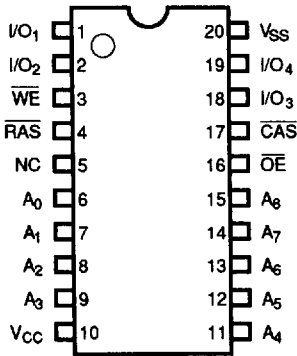
## FEATURES

- 262,144 × 4 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

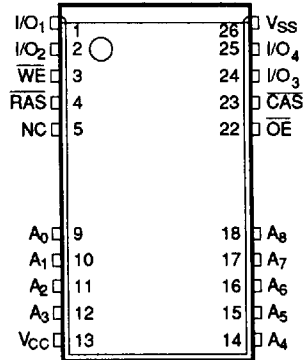
| Parameter   | -40  | -45  | -50  | -60   | -70   |
|---|------|------|------|-------|-------|
| Max. $\overline{\text{RAS}}$ Access Time ( $t_{\text{RAC}}$ ) | 40ns | 45ns | 50ns | 60ns  | 70ns  |
| Max. $\overline{\text{CAS}}$ Access Time ( $t_{\text{CAC}}$ ) | 13ns | 15ns | 15ns | 15ns  | 20ns  |
| Max. Column Address Access Time ( $t_{\text{AA}}$ )           | 25ns | 25ns | 27ns | 30ns  | 35ns  |
| Max. Read/Write Cycle Time ( $t_{\text{RC}}$ )                | 80ns | 80ns | 90ns | 110ns | 130ns |

- Fast Page Mode Operation
- Low Power Operation
  - Low Standby Current (CMOS level inputs)
    - Standard 1mA
    - L version 50µA
- 512 Refresh Cycles
  - Standard distributed across 8ms
  - L version distributed across 128ms
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
  - $\overline{\text{RAS}}$  only
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$
  - Hidden Refresh
- High Reliability Packages
  - Plastic 20pin DIP (P20DP-1A0)
  - Plastic 20pin ZIP (P20ZP-2B0)
  - Plastic 26pin SOJ (P26SJ-2A6)
  - Plastic 24pin TSOP TYPE I (P24TV-5B4)

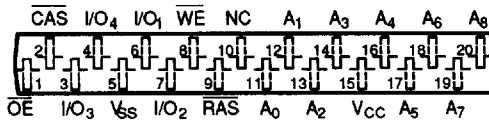
**PIN CONFIGURATION (TOP VIEW)**



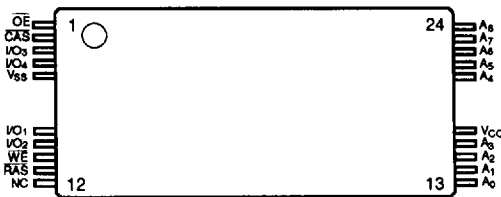
20-pin DIP ( 300mil )  
**P20DP-1A0**



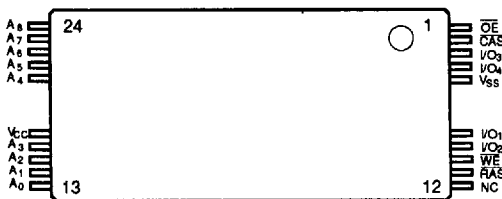
20/26-pin SOJ ( 300mil )  
**P26SJ-2A6**



20-pin ZIP ( 300mil )  
**P20ZP-2B0**



20/24-pin TSOP TYPE ( 1 )  
 Normal Bend (6X16mm)  
**P24TV-5B4**

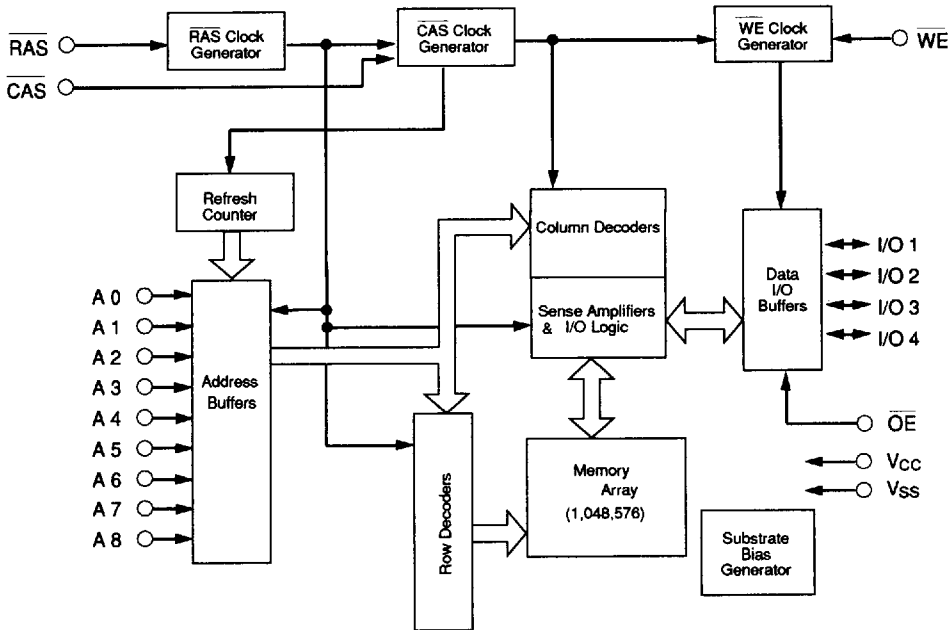


20/24-pin TSOP TYPE ( 1 )  
 Reverse Bend (6X16mm)  
**P24TV-5B4-R**

**PIN NAMES**

|         |                       |
|---------|-----------------------|
| A0-A8   | Address Inputs        |
| RAS     | Row Address Strobe    |
| CAS     | Column Address Strobe |
| OE      | Output Enable         |
| IO1~IO4 | Data-in / Data-out    |
| WE      | Write Enable          |
| VCC     | +5V Supply            |
| VSS     | Ground                |
| NC      | No Connection         |

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| RATING   | SYMBOL                             | VALUE       | UNIT |
|--|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to V <sub>SS</sub>         | V <sub>in</sub> , V <sub>out</sub> | -1 to 7     | V    |
| Voltage on V <sub>CC</sub> Relative to V <sub>SS</sub> | V <sub>CC</sub>                    | -1 to 7     | V    |
| Storage Temperature (Plastic)                          | T <sub>stg</sub>                   | -55 to +125 | °C   |
| Power Dissipation                                      | P <sub>d</sub>                     | 1.0         | W    |
| Ambient Operating Temperature                          | T <sub>a</sub>                     | 0 to +70    | °C   |
| Short Circuit Output Current                           | I <sub>out</sub>                   | 50          | mA   |

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

| SYMBOL          | PARAMETER                      | MIN. | TYP. | MAX. | UNIT |
|-----------------|--------------------------------|------|------|------|------|
| V <sub>CC</sub> | Supply Voltage                 | 4.5  | 5.0  | 5.5  | V    |
| V <sub>SS</sub> | Supply Voltage                 | 0    | 0    | 0    | V    |
| V <sub>IH</sub> | Input High Voltage, All Inputs | 2.4  | —    | 6.5  | V    |
| V <sub>IL</sub> | Input Low Voltage, All Inputs  | -1.0 | —    | 0.8  | V    |

Note: All voltage values in this data sheet are with respect to V<sub>SS</sub> unless otherwise specified.

**NN514256 / NN514256A series**  
**CMOS 256K × 4bit Dynamic RAM**

**DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V<sub>CC</sub> = 5.0V ±10%)**

| SYMBOL           | PARAMETER  | SPEED | MIN. | MAX. | UNIT | TEST CONDITIONS   | NOTES |
|------------------|--|-------|------|------|------|---|-------|
| I <sub>CC1</sub> | Operating Current  | -40   |      | 110  | mA   | t <sub>RC</sub> = t <sub>RC</sub> (min.)<br>RAS, CAS, Address cycling   | 1, 2  |
|                  |  | -45   |      | 100  | mA   |   |       |
|                  |  | -50   |      | 90   | mA   |   |       |
|                  |  | -60   |      | 80   | mA   |   |       |
|                  |  | -70   |      | 70   | mA   |   |       |
| I <sub>CC2</sub> | Standby Current  |       |      | 1.0  | mA   | RAS = CAS ≥ (V <sub>CC</sub> - 0.2V)  |       |
|                  |  |       |      | 2.0  | mA   | RAS = CAS ≥ V <sub>IH</sub>   |       |
| I <sub>CC3</sub> | Refresh Current<br>(RAS only refresh)                      | -40   |      | 110  | mA   | t <sub>RC</sub> = t <sub>RC</sub> (min.)<br>RAS cycling, CAS = V <sub>IH</sub>  | 1     |
|                  |  | -45   |      | 100  | mA   |   |       |
|                  |  | -50   |      | 90   | mA   |   |       |
|                  |  | -60   |      | 80   | mA   |   |       |
|                  |  | -70   |      | 70   | mA   |   |       |
| I <sub>CC4</sub> | Fast Page Mode Current                                     | -40   |      | 80   | mA   | t <sub>PC</sub> = t <sub>PC</sub> (min.)<br>RAS = V <sub>IL</sub><br>CAS, Address cycling   | 1, 2  |
|                  |  | -45   |      | 80   | mA   |   |       |
|                  |  | -50   |      | 70   | mA   |   |       |
|                  |  | -60   |      | 60   | mA   |   |       |
|                  |  | -70   |      | 50   | mA   |   |       |
| I <sub>CC5</sub> | Refresh Current<br>(CAS before RAS refresh)                | -40   |      | 110  | mA   | t <sub>RC</sub> = t <sub>RC</sub> (min.)<br>RAS, CAS cycling  | 1     |
|                  |  | -45   |      | 100  | mA   |   |       |
|                  |  | -50   |      | 90   | mA   |   |       |
|                  |  | -60   |      | 80   | mA   |   |       |
|                  |  | -70   |      | 70   | mA   |   |       |
| I <sub>CC6</sub> | Refresh Current<br>(L version : CAS before<br>RAS refresh) |       |      | 150  | μA   | 512 cycles / 128ms<br>t <sub>RAS</sub> ≤ 200ns, WE ≥ (V <sub>CC</sub> - 0.2V)<br>All other inputs are stable at (V <sub>CC</sub> - 0.2V)<br>or (V <sub>SS</sub> + 0.2V) |       |
| I <sub>L1</sub>  | Input Leakage Current<br>(Any input pin)                   |       | -10  | 10   | μA   | 0V ≤ V <sub>IH</sub> ≤ 5.5V, Others = 0V  |       |
| I <sub>L0</sub>  | Output Leakage Current<br>(For high impedance state)       |       | -10  | 10   | μA   | RAS ≥ V <sub>IH</sub> (min.), CAS ≥ V <sub>IH</sub> (min.)<br>0V ≤ V <sub>OUT</sub> ≤ 5.5V  |       |
| V <sub>OH</sub>  | Output High Voltage  |       | 2.4  |      | V    | I <sub>OH</sub> = -5.0 mA   |       |
| V <sub>OL</sub>  | Output Low Voltage   |       |      | 0.4  | V    | I <sub>OL</sub> = 4.2 mA  |       |

- Notes: 1. I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC5</sub> depend on cycle rate.  
 2. I<sub>CC1</sub> and I<sub>CC4</sub> depend on output loading. Specified values are obtained with the outputs open.

**CAPACITANCE (0°C ≤ Ta ≤ 70°C, V<sub>CC</sub> = 5.0V ±10%, f = 1MHz)**

| SYMBOL           | PARAMETER              | MIN. | MAX. | UNIT |
|------------------|------------------------|------|------|------|
| C <sub>IN1</sub> | Address(A0 ~ A8)       | —    | 5    | pF   |
| C <sub>IN2</sub> | RAS, CAS, WE, OE       | —    | 5    | pF   |
| C <sub>OUT</sub> | I/O1, I/O2, I/O3, I/O4 | —    | 7    | pF   |

**A.C. OPERATING CONDITIONS ( 0 °C ≤ Ta ≤ 70 °C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V ) (NOTES 3, 4, 5)**

| NO. | NOTES                                    |                   | PARAMETER  | -40  |      | -45  |      | -50  |      | -60  |      | -70  |      | UNIT | NOTE  |
|-----|--|-------------------|--|------|------|------|------|------|------|------|------|------|------|------|-------|
|     | JEDEC                                    | STD.              |  | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |      |       |
| 1   | t <sub>CL1QV</sub>                       | t <sub>CAC</sub>  | Access Time from CAS                               | —    | 13   | —    | 15   | —    | 15   | —    | 15   | —    | 20   | ns   | 6,13  |
| 2   | t <sub>CH2QV</sub>                       | t <sub>CPA</sub>  | Access Time from CAS Precharge                     | —    | 30   | —    | 30   | —    | 32   | —    | 35   | —    | 40   | ns   | 13,14 |
| 3   | t <sub>AVQV</sub>                        | t <sub>AA</sub>   | Access Time from Column Address                    | —    | 25   | —    | 25   | —    | 27   | —    | 30   | —    | 35   | ns   | 7,13  |
| 4   | t <sub>RL1QV</sub>                       | t <sub>RAC</sub>  | Access Time from RAS                               | —    | 40   | —    | 45   | —    | 50   | —    | 60   | —    | 70   | ns   | 6,7   |
| 5   | t <sub>RL1CH1</sub>                      | t <sub>CSH</sub>  | CAS Hold Time                                      | 40   | —    | 45   | —    | 50   | —    | 60   | —    | 70   | —    | ns   |       |
| 6   | t <sub>RL1CH1</sub>                      | t <sub>CHR</sub>  | CAS Hold Time (CAS before RAS Refresh)             | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   |       |
| 7   | t <sub>CH2CL2</sub>                      | t <sub>CPN</sub>  | CAS Precharge Time (CAS before RAS Refresh)        | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   |       |
| 8   | t <sub>CH2CL2</sub>                      | t <sub>CPT</sub>  | CAS Precharge Time                                 | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   |       |
| 9   | t <sub>CH2CL2</sub>                      | t <sub>CP</sub>   | CAS Precharge Time (Fast Page Mode)                | 5    | —    | 5    | —    | 5    | —    | 5    | —    | 5    | —    | ns   | 14    |
| 10  | t <sub>CL1CH1</sub>                      | t <sub>CAS</sub>  | CAS Pulse Width                                    | 15   | 100K | 15   | 100K | 15   | 100K | 15   | 100K | 20   | 100K | ns   |       |
| 11  | t <sub>CL1RL2</sub>                      | t <sub>CSR</sub>  | CAS Setup Time (CAS before RAS Refresh)            | 5    | —    | 5    | —    | 5    | —    | 5    | —    | 5    | —    | ns   |       |
| 12  | t <sub>CL1QX</sub>                       | t <sub>CLZ</sub>  | CAS to Output in Low-Z                             | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   | 8     |
| 13  | t <sub>CH2RL2</sub>                      | t <sub>CRP</sub>  | CAS to RAS Precharge Time                          | 5    | —    | 5    | —    | 5    | —    | 5    | —    | 5    | —    | ns   |       |
| 14  | t <sub>CL1WL2</sub>                      | t <sub>CWD</sub>  | CAS to WE Delay Time                               | 45   | —    | 45   | —    | 45   | —    | 45   | —    | 50   | —    | ns   | 11    |
| 15  | t <sub>CL1AX</sub>                       | t <sub>CAH</sub>  | Column Address Hold Time                           | 10   | —    | 10   | —    | 10   | —    | 15   | —    | 15   | —    | ns   |       |
| 16  | t <sub>RL1AX</sub>                       | t <sub>AR</sub>   | Column Address Hold Time Referenced to RAS         | 30   | —    | 30   | —    | 35   | —    | 40   | —    | 40   | —    | ns   |       |
| 17  | t <sub>AVCL2</sub>                       | t <sub>ASC</sub>  | Column Address Setup Time                          | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   | 14    |
| 18  | t <sub>AVRH1</sub>                       | t <sub>RAL</sub>  | Column Address to RAS Lead Time                    | 25   | —    | 25   | —    | 27   | —    | 30   | —    | 35   | —    | ns   |       |
| 19  | t <sub>AVWL2</sub>                       | t <sub>AWD</sub>  | Column Address to WE Delay Time                    | 55   | —    | 55   | —    | 57   | —    | 60   | —    | 65   | —    | ns   | 11    |
| 20  | t <sub>CL1DX</sub><br>t <sub>WL1DX</sub> | t <sub>DH</sub>   | Data Hold Time                                     | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   | 12    |
| 21  | t <sub>DVCL2</sub><br>t <sub>DVWL2</sub> | t <sub>DS</sub>   | Data Setup Time                                    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   | 12    |
| 22  | t <sub>OL1QV</sub>                       | t <sub>OEA</sub>  | OE Access Time                                     | —    | 15   | —    | 15   | —    | 15   | —    | 15   | —    | 20   | ns   |       |
| 23  | t <sub>WL1OL2</sub>                      | t <sub>OEH</sub>  | OE Command Hold Time                               | 15   | —    | 15   | —    | 15   | —    | 15   | —    | 20   | —    | ns   |       |
| 24  | t <sub>CH2QV</sub>                       | t <sub>OED</sub>  | OE to Data Delay Time                              | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   |       |
| 25  | t <sub>CH2QZ</sub>                       | t <sub>OFF</sub>  | Output Buffer Turn-off Delay Time                  | 0    | 13   | 0    | 13   | 0    | 13   | 0    | 15   | 0    | 20   | ns   | 10    |
| 26  | t <sub>OH2QX</sub>                       | t <sub>OEZ</sub>  | Output Buffer Turn-off Delay Time Referenced to OE | 0    | 10   | 0    | 10   | 0    | 10   | 0    | 15   | 0    | 15   | ns   |       |
| 27  | t <sub>CL1RH1</sub>                      | t <sub>RSH</sub>  | RAS Hold Time                                      | 15   | —    | 15   | —    | 15   | —    | 15   | —    | 20   | —    | ns   |       |
| 28  | t <sub>OL1RH1</sub>                      | t <sub>ROH</sub>  | RAS Hold Time Referenced to OE                     | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   |       |
| 29  | t <sub>RH2RL2</sub>                      | t <sub>RP</sub>   | RAS Precharge Time                                 | 25   | —    | 25   | —    | 25   | —    | 30   | —    | 40   | —    | ns   |       |
| 30  | t <sub>RL1RH1</sub>                      | t <sub>RAS</sub>  | RAS Pulse Width                                    | 40   | 100K | 45   | 100K | 50   | 100K | 60   | 100K | 70   | 100K | ns   |       |
| 31  | t <sub>RL1RH1</sub>                      | t <sub>RASP</sub> | RAS Pulse Width (Fast Page Mode)                   | 40   | 100K | 45   | 100K | 50   | 100K | 60   | 100K | 70   | 100K | ns   |       |
| 32  | t <sub>RL1CL1</sub>                      | t <sub>RCD</sub>  | RAS to CAS Delay Time                              | 13   | 25   | 13   | 30   | 13   | 35   | 13   | 45   | 13   | 50   | ns   | 6     |
| 33  | t <sub>RH2CL2</sub>                      | t <sub>RPC</sub>  | RAS to CAS Precharge Time                          | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   |       |
| 34  | t <sub>RL1AV</sub>                       | t <sub>RAD</sub>  | RAS to Column Address Delay Time                   | 11   | 15   | 11   | 20   | 11   | 23   | 11   | 30   | 11   | 35   | ns   | 7     |
| 35  | t <sub>RL1WL2</sub>                      | t <sub>RWD</sub>  | RAS to WE Delay Time                               | 70   | —    | 75   | —    | 80   | —    | 90   | —    | 100  | —    | ns   | 11    |
| 36  | t <sub>CH2WL2</sub>                      | t <sub>RCH</sub>  | Read Command Hold Time                             | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   | 9     |
| 37  | t <sub>RH2WL2</sub>                      | t <sub>RRH</sub>  | Read Command Hold Time Referenced to RAS           | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 10   | —    | ns   | 9     |
| 38  | t <sub>WH2CL2</sub>                      | t <sub>RCS</sub>  | Read Command Setup Time                            | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   |       |

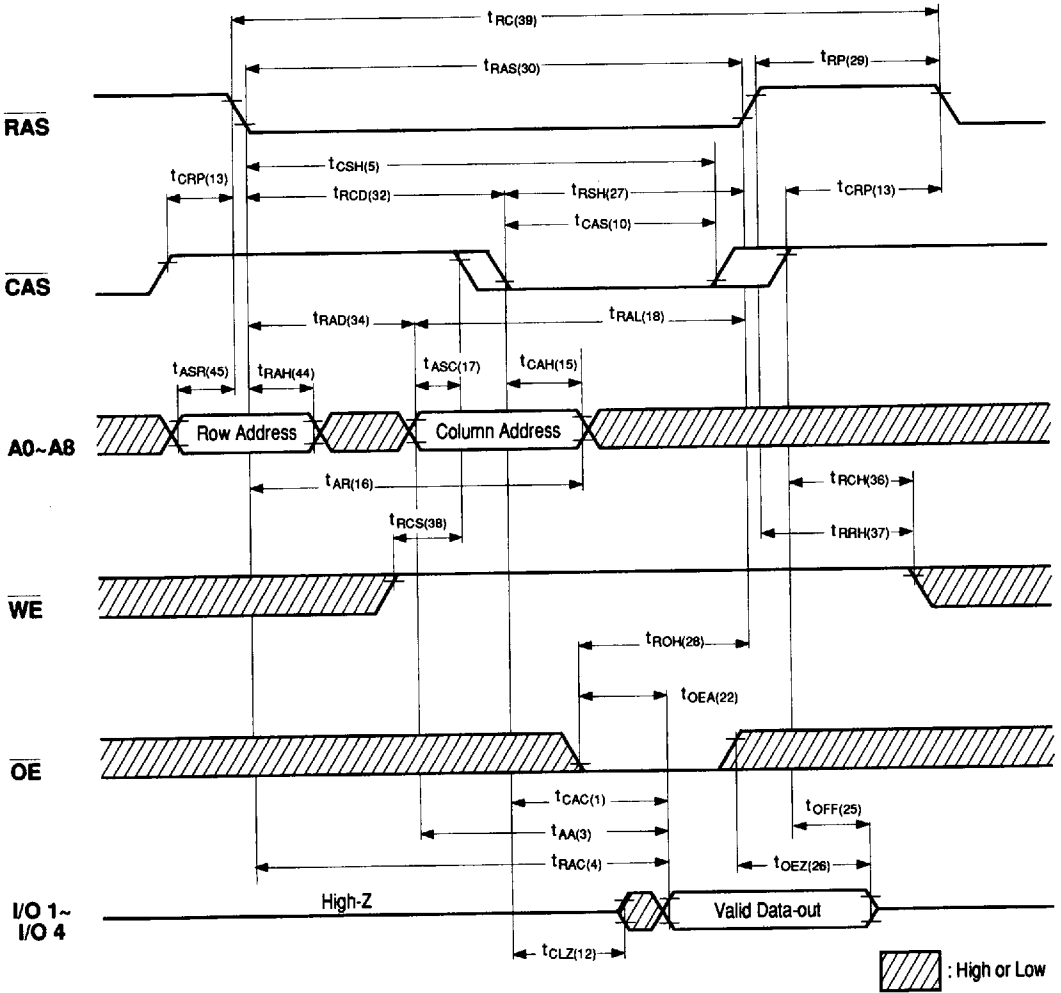
**NN514256 / NN514256A series**  
**CMOS 256K × 4bit Dynamic RAM**

| NO. | SYMBOL              |                   | PARAMETER  | -40  |      | -45  |      | -50  |      | -60  |      | -70  |      | UNIT | NOTE  |
|-----|---------------------|-------------------|--|------|------|------|------|------|------|------|------|------|------|------|-------|
|     | JEDEC               | STD.              |  | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |      |       |
| 39  | t <sub>RL2RL2</sub> | t <sub>RC</sub>   | Random Read or Write Cycle Time                    | 80   | —    | 80   | —    | 90   | —    | 110  | —    | 130  | —    | ns   |       |
| 40  | t <sub>CL2CL2</sub> | t <sub>PC</sub>   | Read or Write Cycle Time (Fast Page Mode)          | 30   | —    | 30   | —    | 33   | —    | 40   | —    | 45   | —    | ns   | 13,14 |
| 41  | t <sub>RL2RL2</sub> | t <sub>RMW</sub>  | Read-Modify-Write Cycle Time                       | 130  | —    | 135  | —    | 145  | —    | 165  | —    | 185  | —    | ns   |       |
| 42  | t <sub>CL2CL2</sub> | t <sub>PRMW</sub> | Read-Modify-Write Cycle Time (Fast Page Mode)      | 85   | —    | 90   | —    | 90   | —    | 95   | —    | 100  | —    | ns   | 13,14 |
| 43  | t <sub>REF</sub>    | t <sub>REF</sub>  | Refresh Period                                     | —    | 8    | —    | 8    | —    | 8    | —    | 8    | —    | 8    | ms   | 15    |
| 44  | t <sub>RL1AX</sub>  | t <sub>RAH</sub>  | Row Address Hold Time                              | 8    | —    | 8    | —    | 8    | —    | 8    | —    | 8    | —    | ns   |       |
| 45  | t <sub>AVRL2</sub>  | t <sub>ASR</sub>  | Row Address Setup Time                             | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   |       |
| 46  | t <sub>T</sub>      | t <sub>T</sub>    | Transition Time (Rise and Fall)                    | 2    | 50   | 2    | 50   | 2    | 50   | 2    | 50   | 2    | 50   | ns   | 4,5   |
| 47  | t <sub>CL1WH1</sub> | t <sub>WCH</sub>  | Write Command Hold Time                            | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 15   | —    | ns   |       |
| 48  | t <sub>WL1WH1</sub> | t <sub>WP</sub>   | Write Command Pulse Width                          | 10   | —    | 10   | —    | 10   | —    | 10   | —    | 15   | —    | ns   |       |
| 49  | t <sub>WL1CL2</sub> | t <sub>WCS</sub>  | Write Command Setup Time                           | 0    | —    | 0    | —    | 0    | —    | 0    | —    | 0    | —    | ns   | 11    |
| 50  | t <sub>WL1CH1</sub> | t <sub>CWL</sub>  | Write Command to $\overline{\text{CAS}}$ Lead Time | 10   | —    | 15   | —    | 15   | —    | 15   | —    | 20   | —    | ns   |       |
| 51  | t <sub>WL1RH1</sub> | t <sub>RWL</sub>  | Write Command to $\overline{\text{RAS}}$ Lead Time | 10   | —    | 15   | —    | 15   | —    | 15   | —    | 20   | —    | ns   |       |

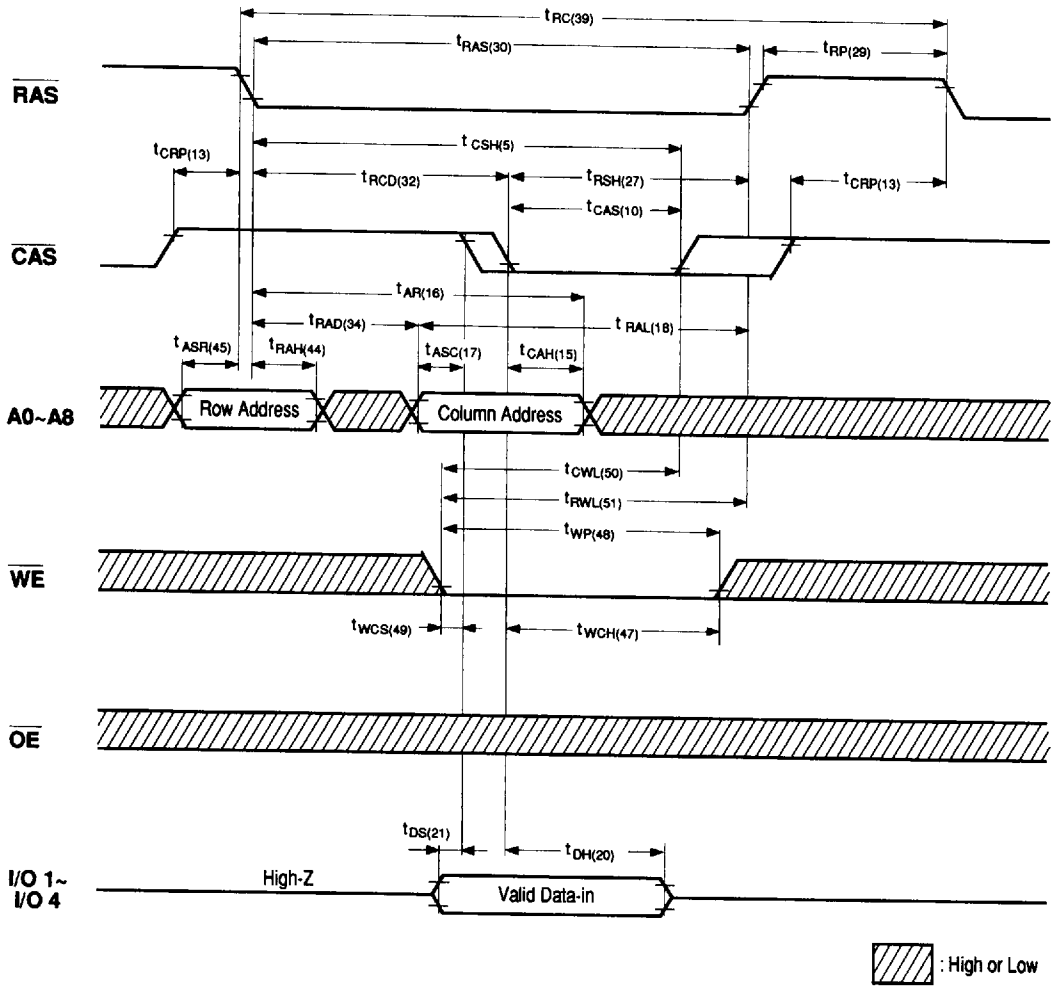
**Notes:**

- Eight Initialization Cycles are required following a 200 $\mu$ s pause after Power Up. These Initialization Cycles may consist of one of the following :  $\overline{\text{RAS}}$  only refresh Cycles, Read Cycles, Write Cycles,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh Cycles.
- AC measurements assume  $t_T=3\text{ns}$ . All AC parameters are measured with  $V_{IL}(\text{min.}) \geq V_{SS}$  and  $V_{IH}(\text{max.}) \leq V_{CC}$  and with a load equivalent to two TTL loads and 100pF.
- $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
- Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
- Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
- Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- $t_{OFF}(\text{max.})$  defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in read-modify-write cycles.
- Access time is determined by the longer of  $t_{AA}$ ,  $t_{CAC}$ , or  $t_{CPA}$ .
- $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\text{min.})$  and  $t_{CPA}(\text{max.})$  values.
- $t_{REF}=128\text{msec}$  for Long Refresh version (L version).

READ CYCLE

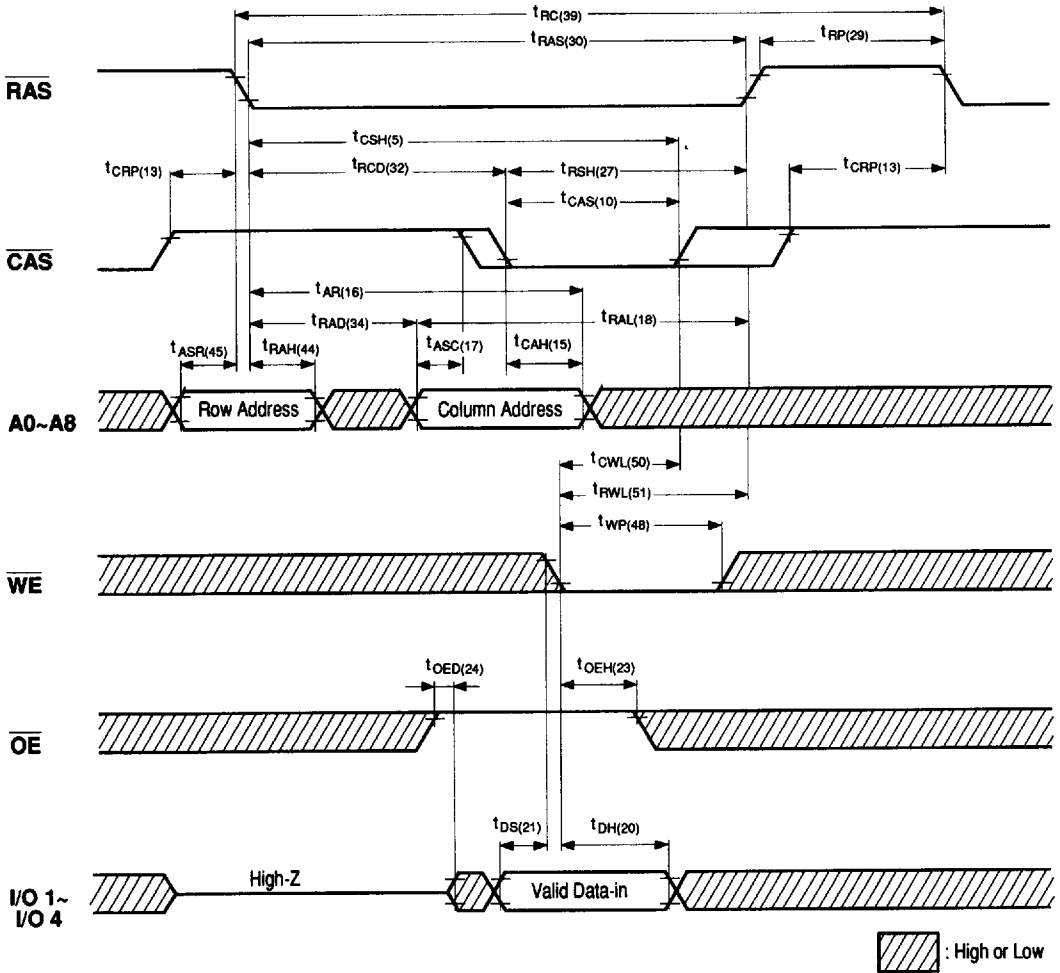


**WRITE CYCLE (EARLY WRITE)**

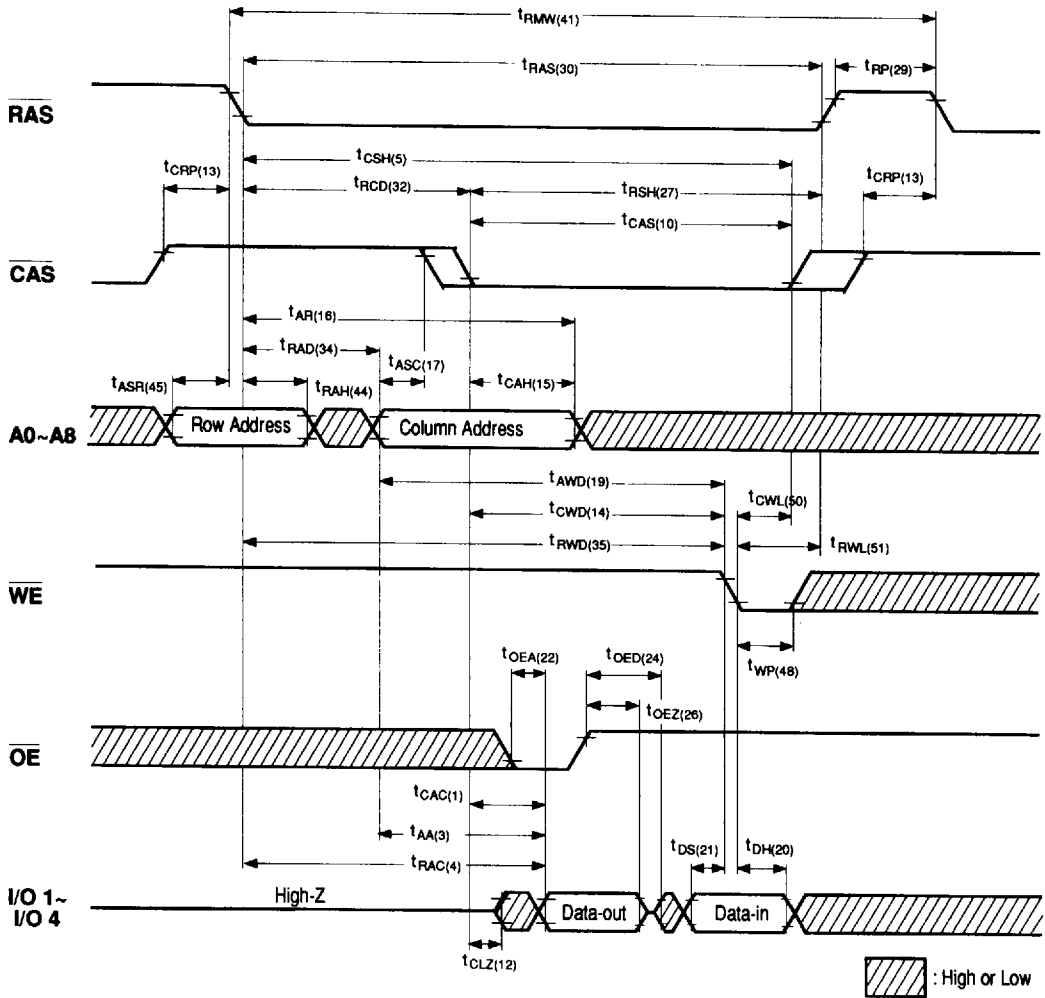




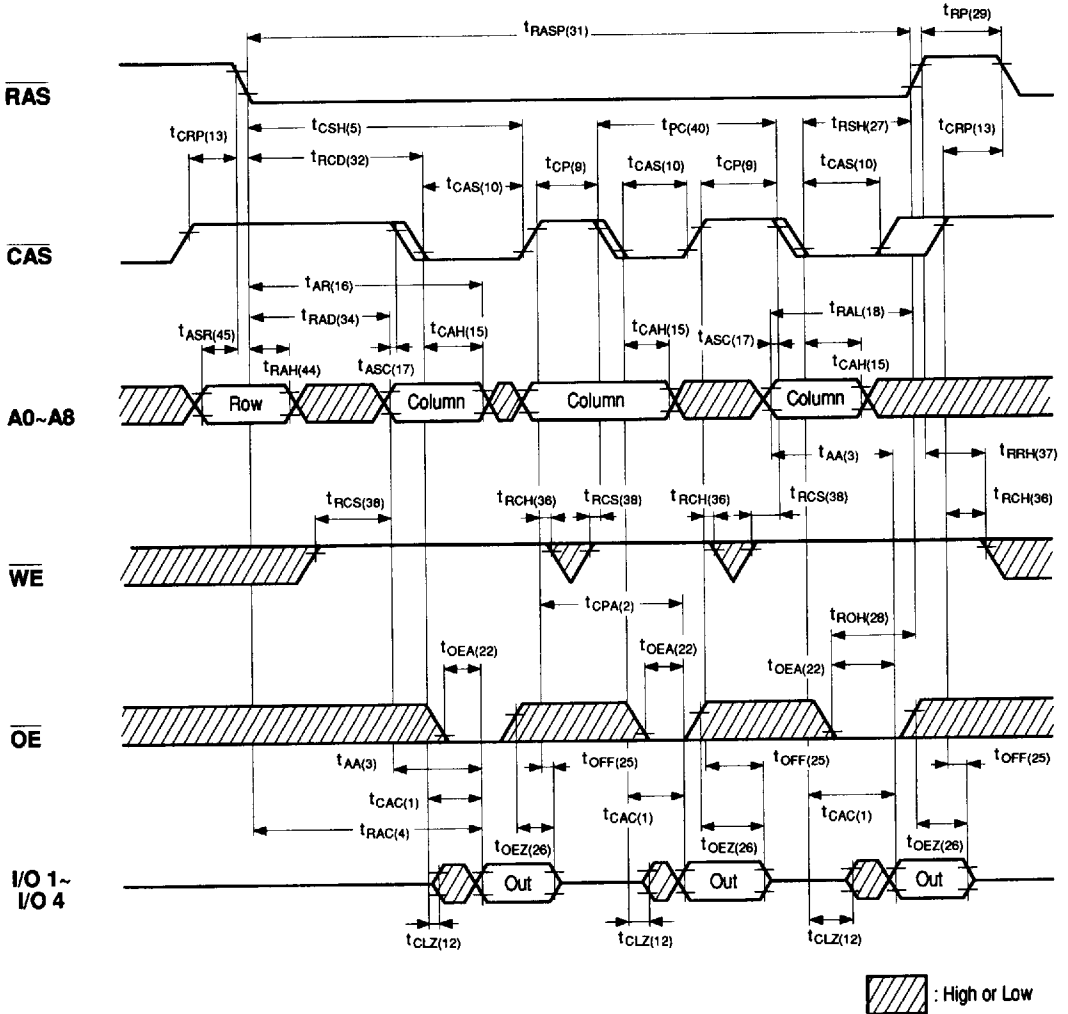
WRITE CYCLE ( $\overline{OE}$ -CONTROLLED WRITE)



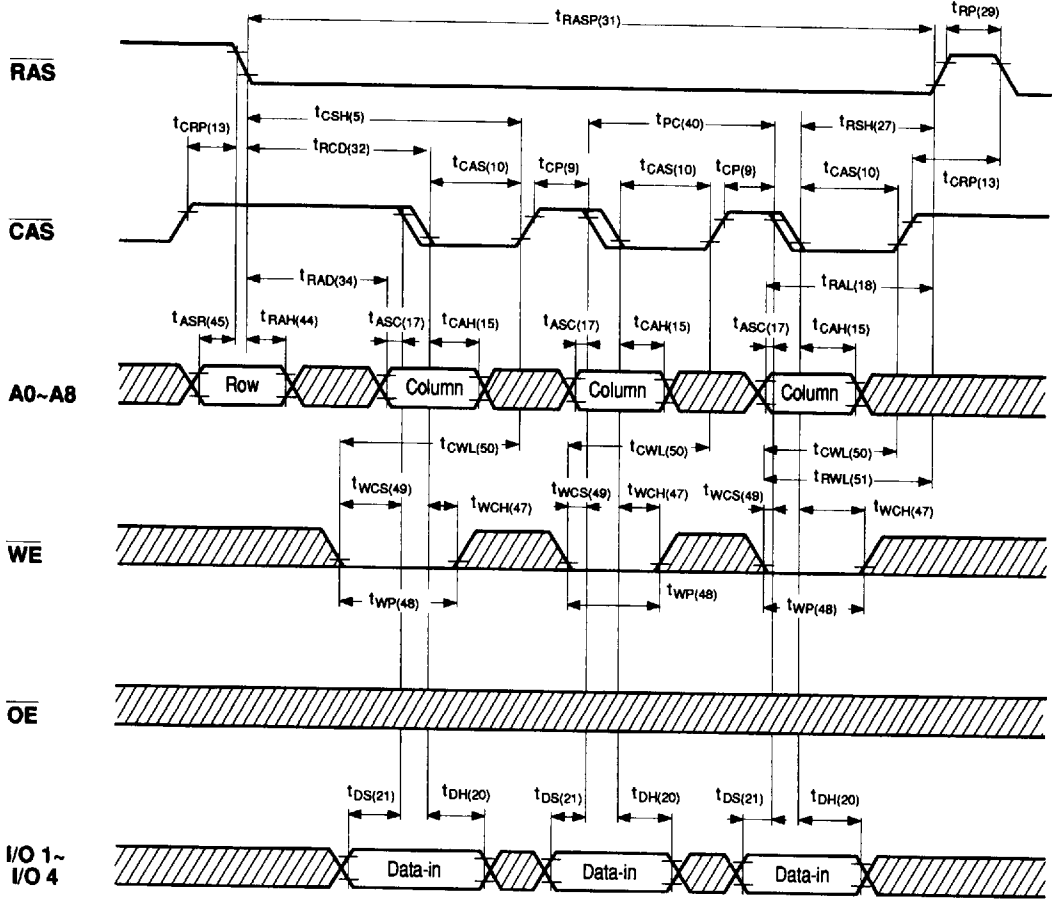
**READ-MODIFY-WRITE CYCLE**



FAST PAGE MODE READ CYCLE

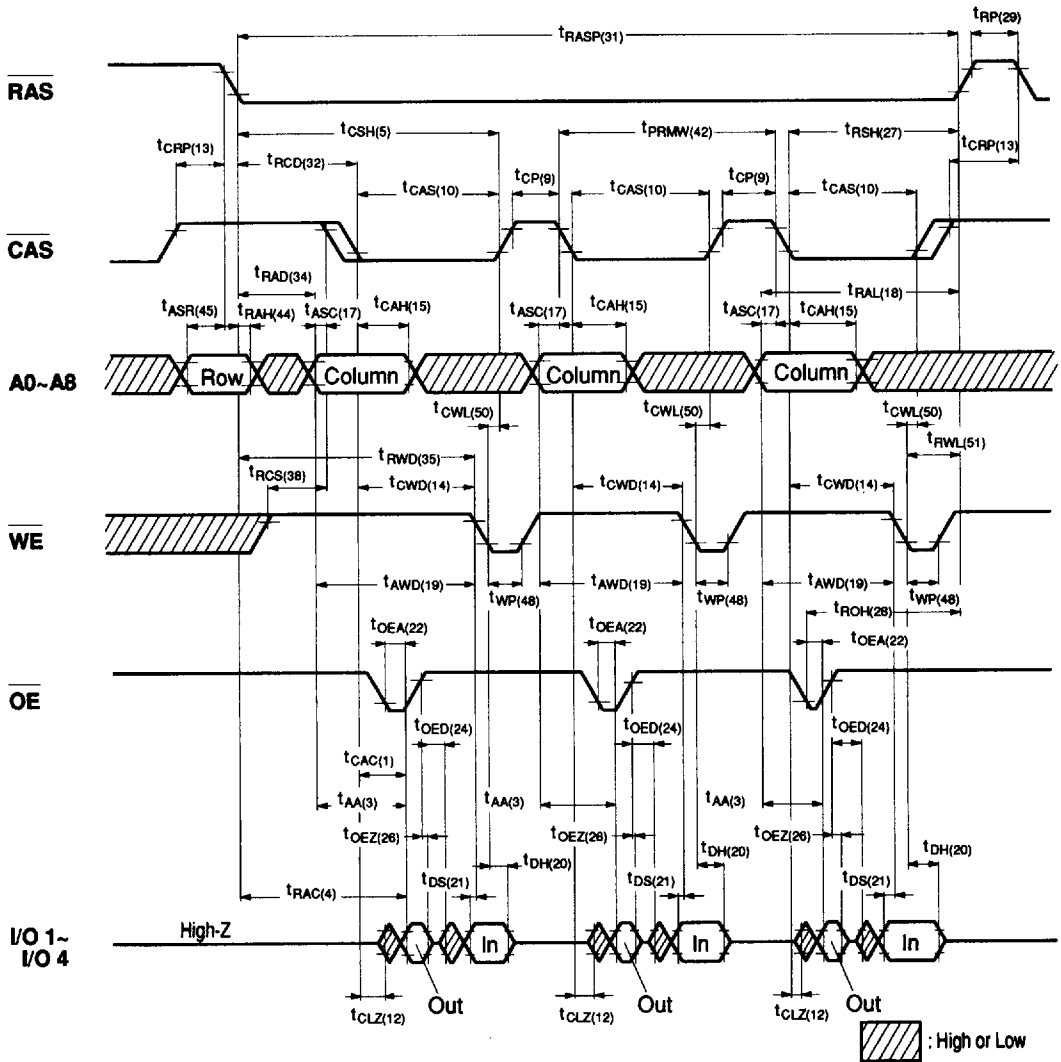


**FAST PAGE MODE EARLY WRITE CYCLE**

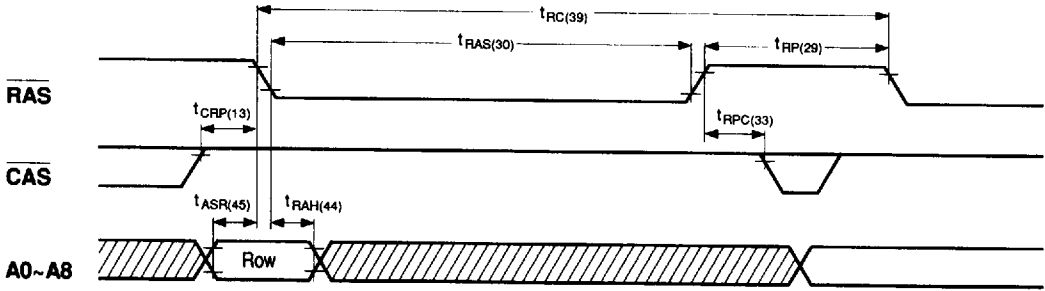


 : High or Low

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



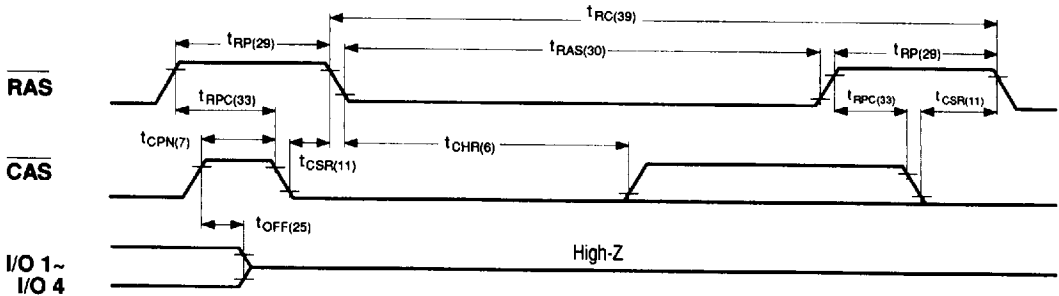
**RAS ONLY REFRESH CYCLE**



Note:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  = Don't care.

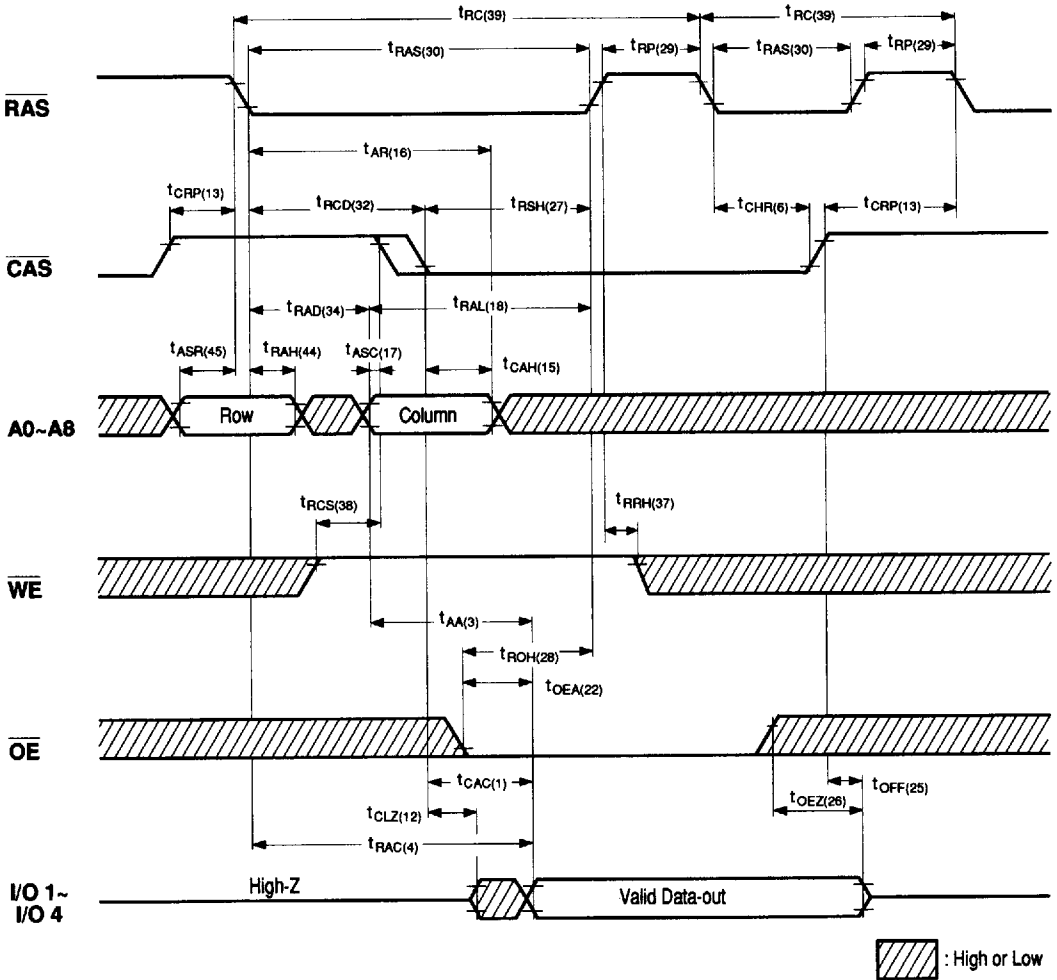
 : High or Low

**CAS BEFORE RAS REFRESH CYCLE**

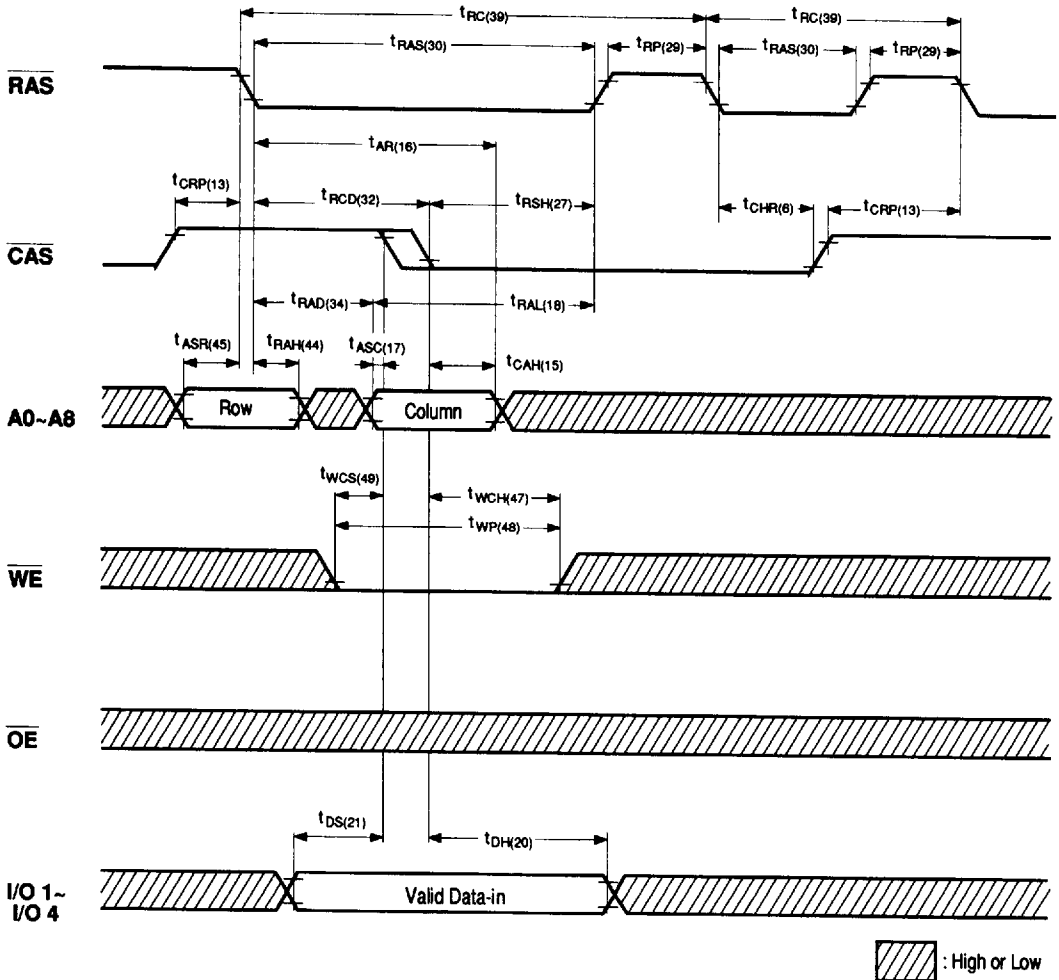


Note:  $\overline{\text{OE}}$ ,  $\text{A0} \sim \text{A8}$  = Don't care.

HIDDEN REFRESH CYCLE (READ)



**HIDDEN REFRESH CYCLE (EARLY WRITE)**





**ORDERING INFORMATION**

**NN514256XXX - XX**

